Electronic Version
Stylesheet Version v1.1.1

Reducing Number of Pins Required to Test Integrated Circuits

Abstract

Number of pins required to test integrated circuits are reduced by scanning in a sequence of bits sequentially on a pin. The scanned bits are shifted into a shift register, and then loaded into a select register. The bit values in the select register represent the set of tests desired to be performed, and the desired tests can accordingly be performed within the integrated circuit. As bits representing the desired tests can be scanned using a small number of pins, the aggregate number of pins required for testing may be reduced.